[0280] In other periods, excluding the i-th period HPi, the first clock signal CKV of the high level VH-C output from the second inverter transistor T**7** is provided to the second node A.

[0281] A voltage of the i-th gate signal G[i] after the (i+1)-th period HP(i+1) corresponds to a voltage of the output terminal OUT. During the (i+1)-th period HP(i+1), the first pull-down transistor T**2** provides the first ground voltage VSS**1** to the output terminal OUT in response to the (i+1)-th carry signal.

[0282] A voltage of the i-th carry signal CR[i] after the (i+1)-th period HP(i+1) corresponds to a voltage of the carry terminal CR. During the (i+1)-th period HP(i+1), the second pull-down transistor T**17** provides the second ground voltage VSS**2** to the carry terminal CR in response to the (i+1)-th carry signal.

[0283] After the (i+1)-th period HP(i+1), the first holding transistor T**3** provides the first ground voltage VSS**1** to the output terminal OUT in response to a switching signal output from the second node A.

[0284] After the (i+1)-th period HP(i+1), the second holding transistor T**11** provides the second ground voltage VSS**2** to the carry terminal CR in response to a switching signal output from the second node A.

[0285] Next, an alternative exemplary embodiment of the driving stage of FIG. **14** will be described with reference to FIG. **17**.

[0286] FIG. **17** is a circuit diagram of an alternative exemplary embodiment of a driving stage of FIG. **14**. In an exemplary embodiment, as show in FIG. **17**, the i-th driving stage SRCi'**2** includes output units **810-1** and **810-2**, a controller **820**, an inverter **830**, pull-down units **840-1** and **840-2**, and holding units **850-1** and **850-2**.

[0287] The circuit diagram in FIG. **17** is substantially the same as the circuit diagram shown in FIG. **15**, except for a connection structure of a third inverter transistor T**13** included in the inverter **830**, and any repetitive detailed description of same or like elements will hereinafter be omitted or simplified.

[0288] In such an embodiment, the inverter **830** outputs a switching signal to the second node A. The inverter **830** includes first to fourth inverter transistors T**12**, T**7**, T**13** and T**8**. Among the first to fourth inverter transistors T**12**, T**7**, T**13** and T**8**, the first, second and fourth transistors T**12**, T**7** and T**8** are the same as the first, second and fourth transistors T**12**, T**7**, and T**8** of the inverter **730** of FIG. **15**, and any repetitive detailed description thereof will be omitted.

[0289] In such an embodiment, the third inverter transistor T**13** includes an output end connected to an output end of the first inverter transistor T**12**, a control end connected to a carry terminal CR, and an input end connected to a first ground terminal V**1**.

[0290] In such an embodiment, a leakage current of the third inverter transistor T**13** due to a ripple generated from the carry terminal CR may be reduced by reducing a potential difference V_{GS} between the input end and the control end of the third inverter transistor T**13**.

[0291] While the invention has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. A gate driving circuit comprising:

a plurality of stages which outputs gate signals to corresponding gate lines, respectively,

wherein a stage of the plurality of stages comprises:

a first control transistor diode-connected between a first input end of the stage and a first node, wherein the first control transistor is biased by a first input signal of the first input end of the stage, and back-biased by a second input signal of a second input end of the stage;

a second control transistor comprising a control end connected to a third input end of the stage and which receives a third input signal, a first end connected to the first node, and a second end connected to a first voltage, wherein the second control transistor is back-biased by a fourth input signal of a fourth input end of the stage;

a first output transistor comprising a control end connected to the first node, a first end connected to a clock input end of the stage, and a second end connected to a first output end of the stage; and

a capacitor connected between the control end of the first output transistor and the second end of the first output transistor,

wherein the second input signal and the fourth input signal have enable levels during different periods from each other.

2. The gate driving circuit of claim **1**, wherein the stage of the plurality of stages further comprises:

a second output transistor comprising a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a second output end of the stage to output a carry signal; and

a third output transistor comprising a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a third output end of the stage to output a compensation signal,

wherein the second output transistor is back-biased by the compensation signal.

3. The gate driving circuit of claim **2**, wherein the second input signal is a compensation signal output from a previous stage of the stage, among the plurality of stages.

4. The gate driving circuit of claim **2**, wherein the fourth input signal is a compensation signal output from a next stage of the stage, among the plurality of stages.

5. The gate driving circuit of claim **2**, wherein the stage of the plurality of stages further comprises:

an inverter which outputs a signal synchronized to a clock signal of the clock input end to a second node during a period other than a period during which the carry signal is output; and

holding units which provide a back-bias voltage to the third output end in response to a signal output from the second node.

6. The gate driving circuit of claim **5**, wherein the inverter comprises at least two transistors connected to a first voltage having a lower voltage level than a low level of the gate signals.

7. The gate driving circuit of claim **6**, wherein the at least two transistors are back-biased by one of the back-bias voltage or the compensation signal.